IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Constantin Bulucea and Rebecca Rossen

Assignee: Siliconix Incorporated

Title: TRENCH DMOS POWER TRANSISTOR WITH FIELD-SHAPING PROFILE AND THREE-DIMENSIONAL GEOMETRY

Serial No.: 08/086,976 Filed: 7/2/93

Examiner: J. Carroll Group Art Unit: 2508

Attorney Docket No.: M-799-2D US

San Jose, California
March 17, 1994

COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D. C. 20231

Declaration of Constantin Bulucea

Sir:

I, Constantin Bulucea, hereby declare:

1. I am an inventor of claims 17-29 of the above-mentioned Application and inventor of the subject matter described and claimed therein (collectively, the "Subject Matter").

2. I conceived the Subject Matter prior to August 24, 1988. In support of my conception date prior to August 24, 1988, I enclose Exhibit A, which includes Figures 1-10 and 21-31A of the above-mentioned Application. Exhibit A, which shows the Subject Matter and bears the signatures of Messr. Richard K. Williams and Randolph D. Mah, are signed respectively on August 10, 1988 and August 11, 1988 in my presence.

3. Between August 11, 1988 and October 3, 1988, I worked with Mr. Lorimer K. Hill, then Patent Coordinator of Siliconix Incorporated, to obtain Siliconix's approval for an application for patent. As evidence of this effort, I enclose a letter (Exhibit B) from Mr. Hill to Mr. Paul Winters, a partner of the law firm Skjerven, Morrill, MacPherson Franklin and Friel

LAW OFFICES OF
SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

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("Skjerven Morrill"), instructing Mr. Winters to prepare an application for patent in the United States.

3. Between October 3, 1988 and December 27, 1988, I worked diligently with my attorney Mr. John F. Schipper, who was then associated with Skjerven Morrill, to prepare a patent application. The patent application became U.S. Patent Application, serial no. 07/290,546, filed on December 27, 1988, issued on December 10, 1991 as U.S. Patent 5,072,266, from which the parent Application (serial no. 07/762,103, filed on 9/18/91) of the present Application based priority under 35 U.S.C. § 120 .

4. I did not abandon the Subject Matter at any time between my conception of the Subject Matter and December 27, 1988.

Respectfully submitted,

MAR 17 1994

Constantin Bulucea

Constantin Bulucea

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on 3/17 1994

3/17/94
Date of Signature

Attorney(s) for Applicant(s)

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MacPHERSON, FRANKLIN
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EXHIBIT A

#6

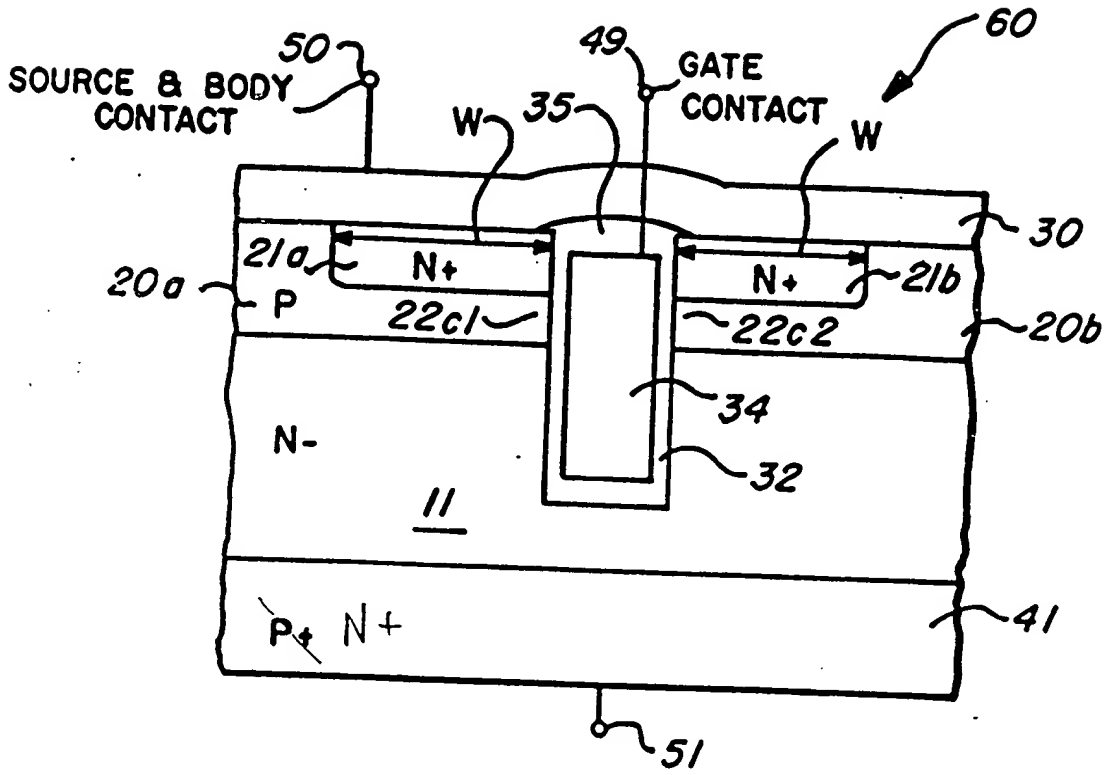


Figure 1

Cross-section of a trenched DMOS power transistor cell (prior art, /1,2/).

read understood August 10, 1988

read and understood Ronald D. Mesh August 11, 1988

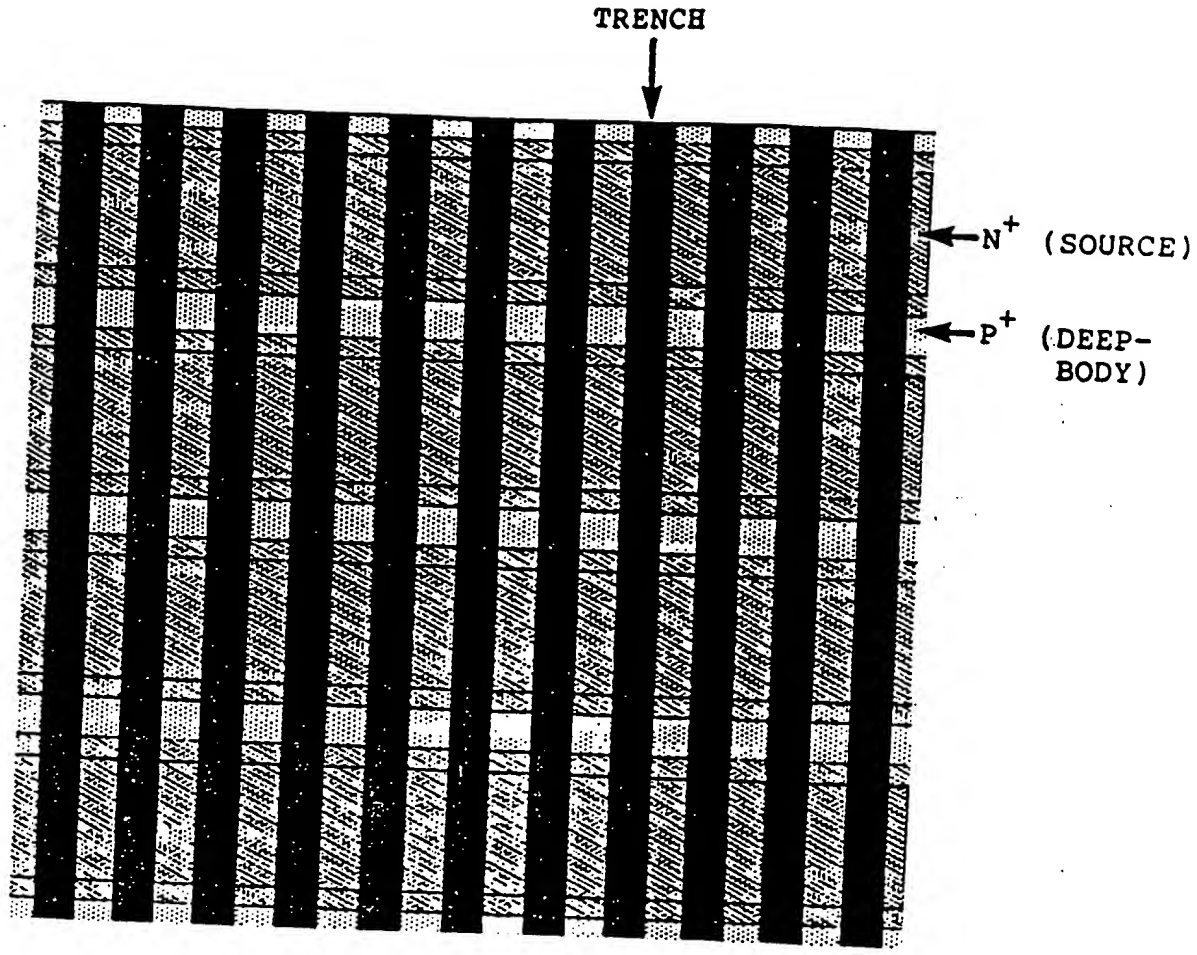


Figure 2,a

"Open-cell" implementation of a trenched DMOS power transistor (CALMA hard copy, active region). Siliconix, Inc., 1987.

read + understood OK WH August 10, 1988
read and understood Rudolph D. Mak August 11, 1988

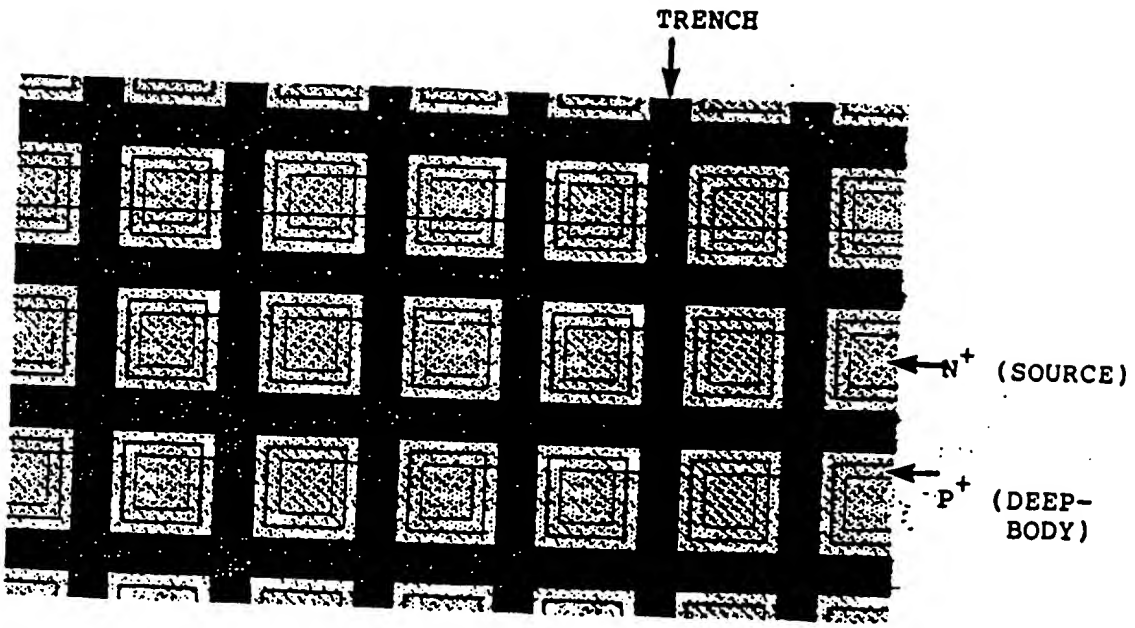


Figure 2,b

"Closed-cell" implementation of a trenched DMOS power transistor (CALMA hard copy, active region). Siliconix, Inc., 1987.

read + understood August 10, 1988
read and understood August 4, 1988

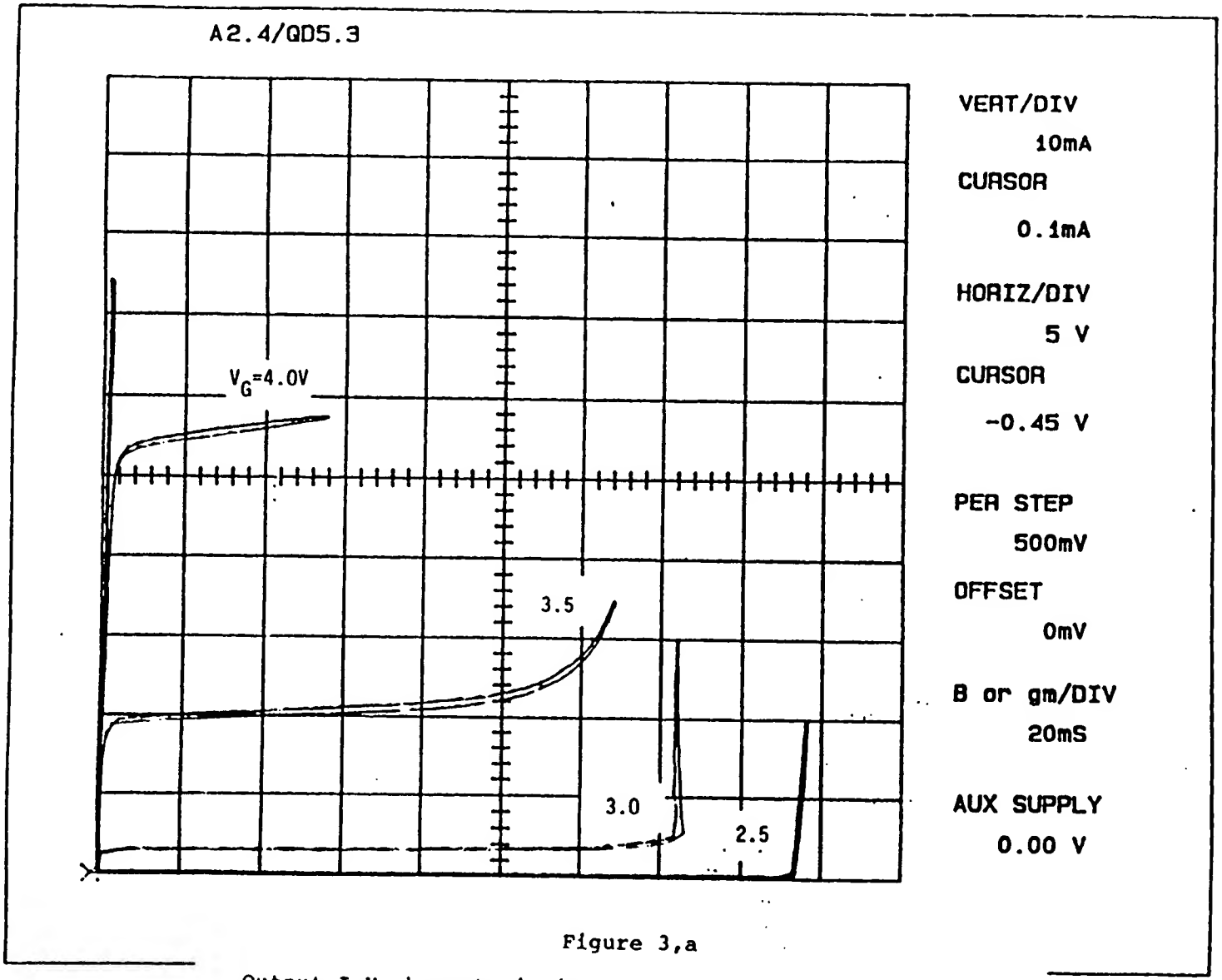


Figure 3,a

Output I-V characteristics of an experimental "open-cell" trenched DMOS transistor having distant body contacts, perpendicular to the trenches. Siliconix, Inc., 1988.

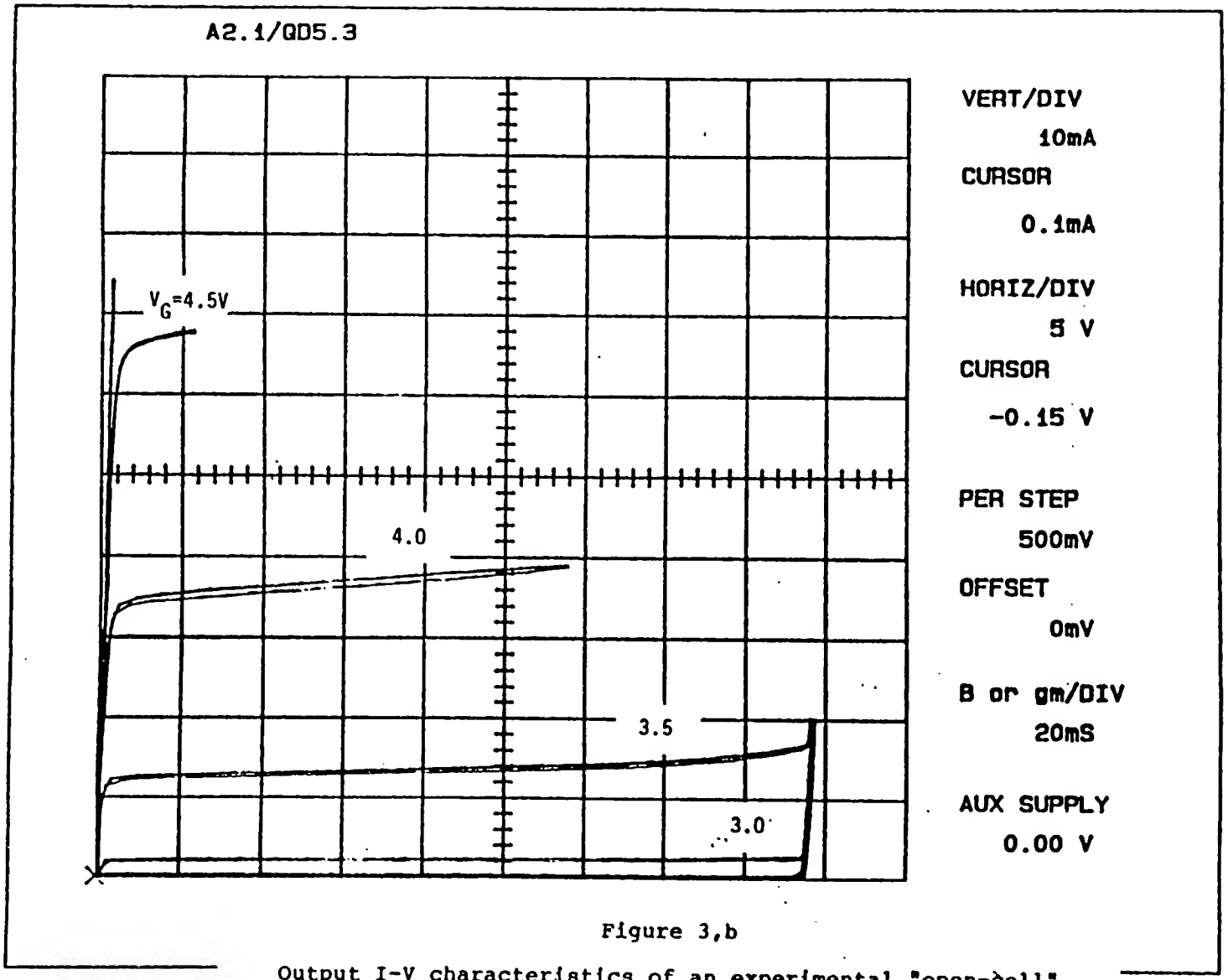


Figure 3,b

Output I-V characteristics of an experimental "open-cell" trenched DMOS transistor having closely-spaced body contacts, perpendicular to the trenches. Siliconix, Inc., 1988.

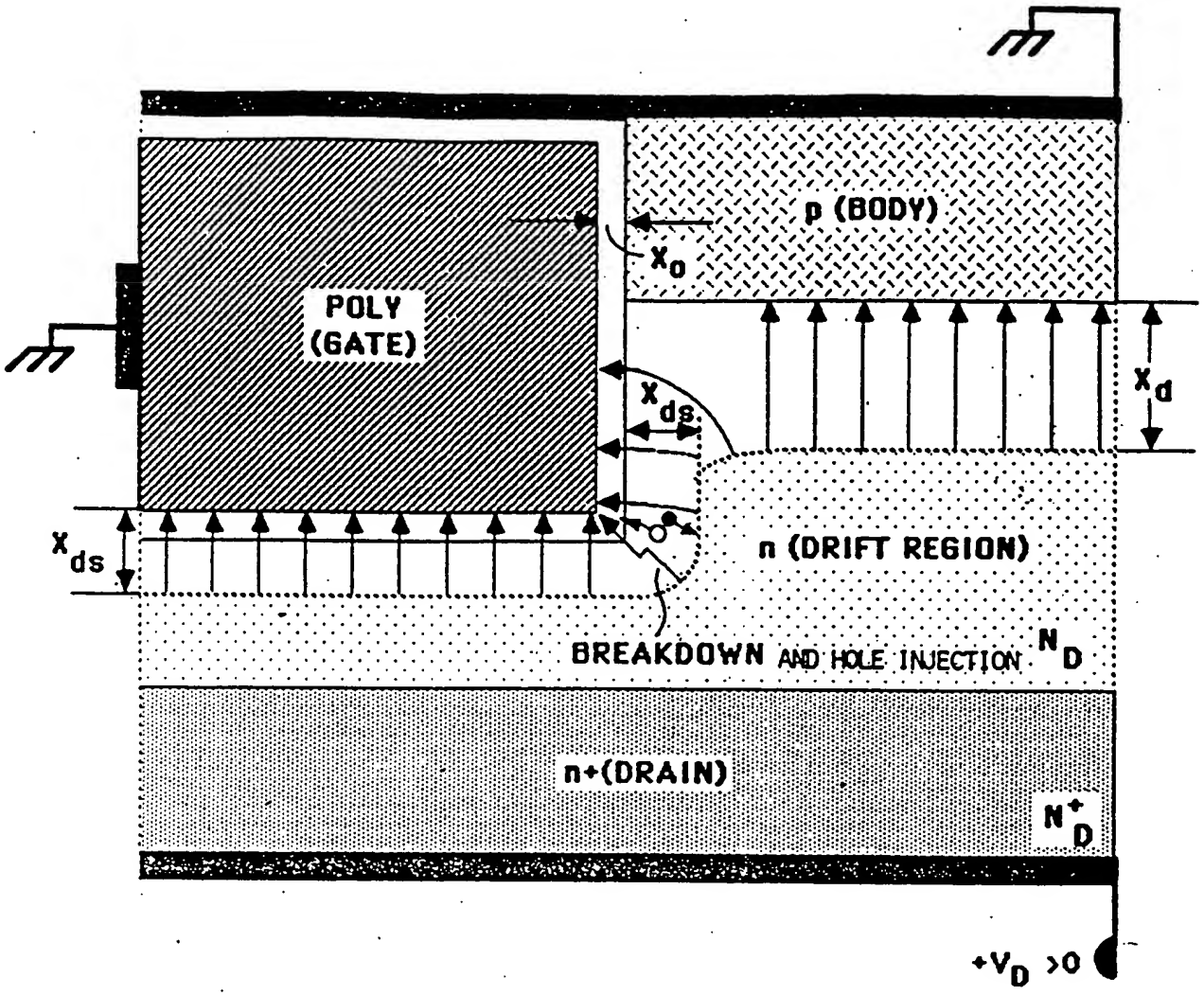


Figure 4

Qualitative description of the electric-field structure in a trenched DMOS transistor having no deep-body profile provision. BVDSS biasing, source junction omitted.

read & understood August 10, 1988
read and understood August 11, 1988

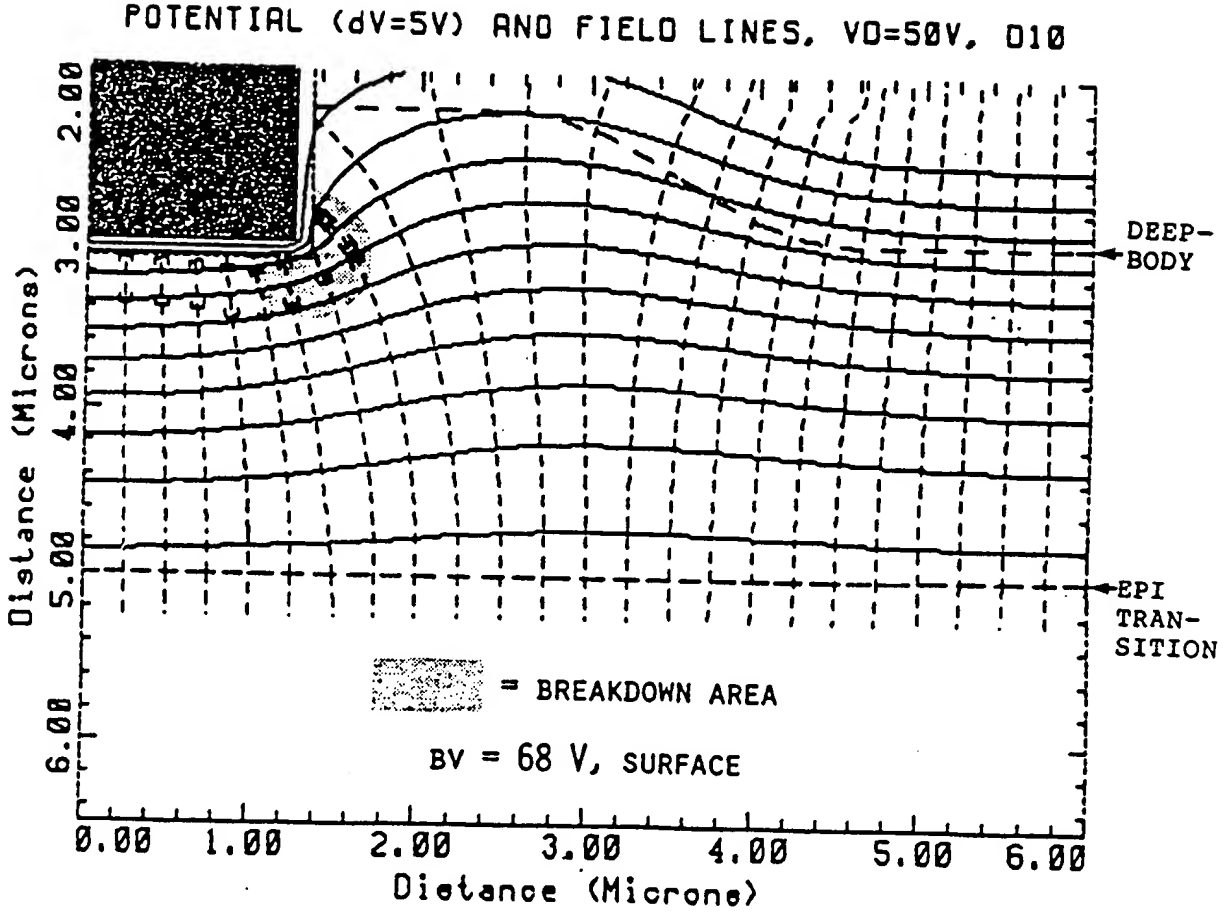


Figure 5

2-D computer simulation of the BVDSS operation of a trenched DMOS transistor having the deep body junction shallower than the trench. Drain breakdown takes place beneath the trench surface.

read & understood August 10, 1988
read & understood August 11, 1988

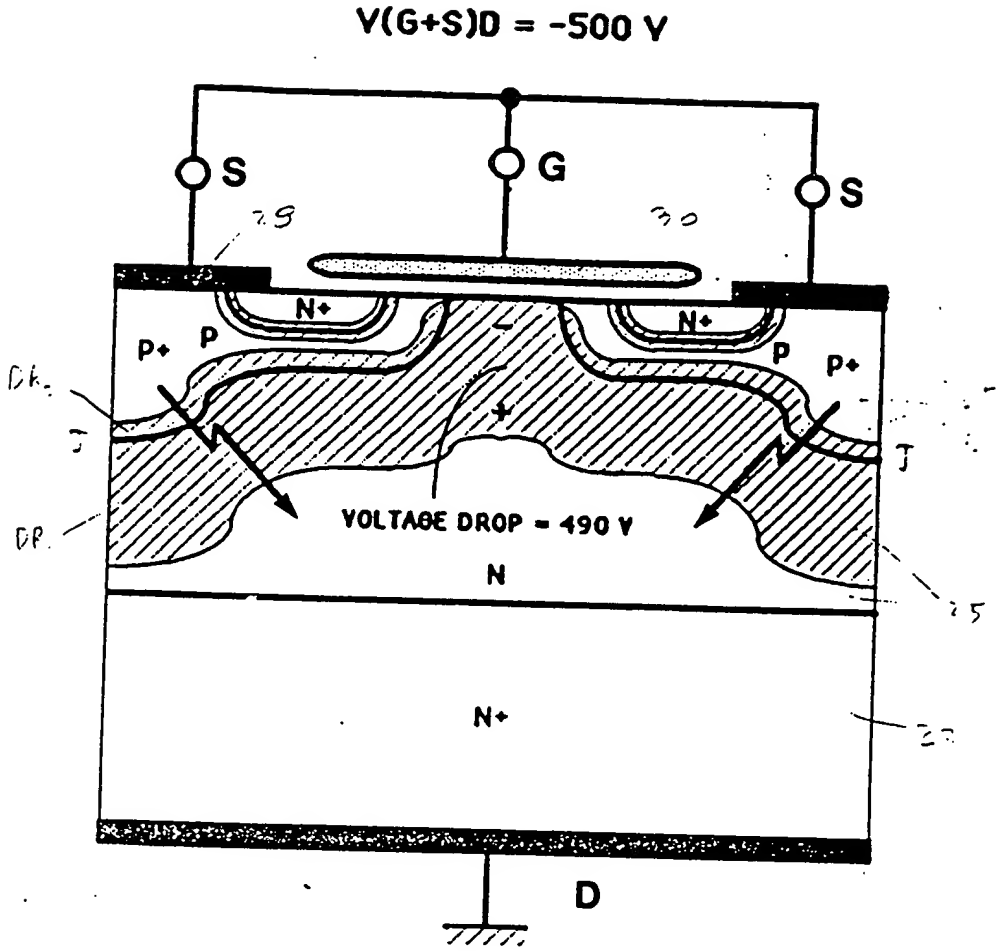


Figure 6

Junction and depletion-region topology of a planar DMOS transistor biased in the BVDSS condition.

read + understood August 10, 1988
read & understood Rachel D. M. August 11, 1988

2-D OXIDATION
SQUARE-CELL DESIGN

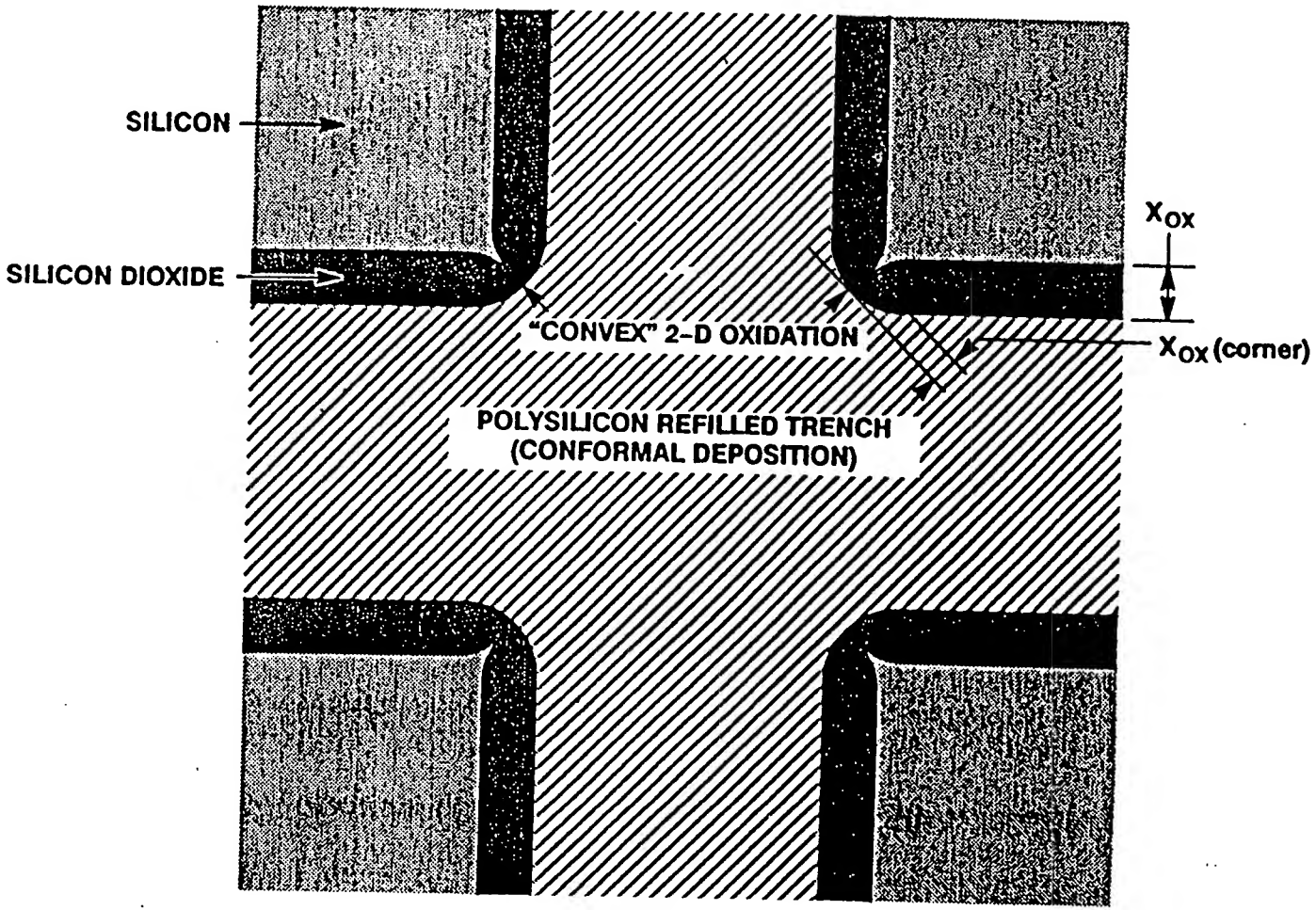


Figure 7

Qualitative description of the oxide profile at a rectangular trench intersection.

read + understood QKWA August 10, 1988
read and understood Ralph Dill August 4, 1988

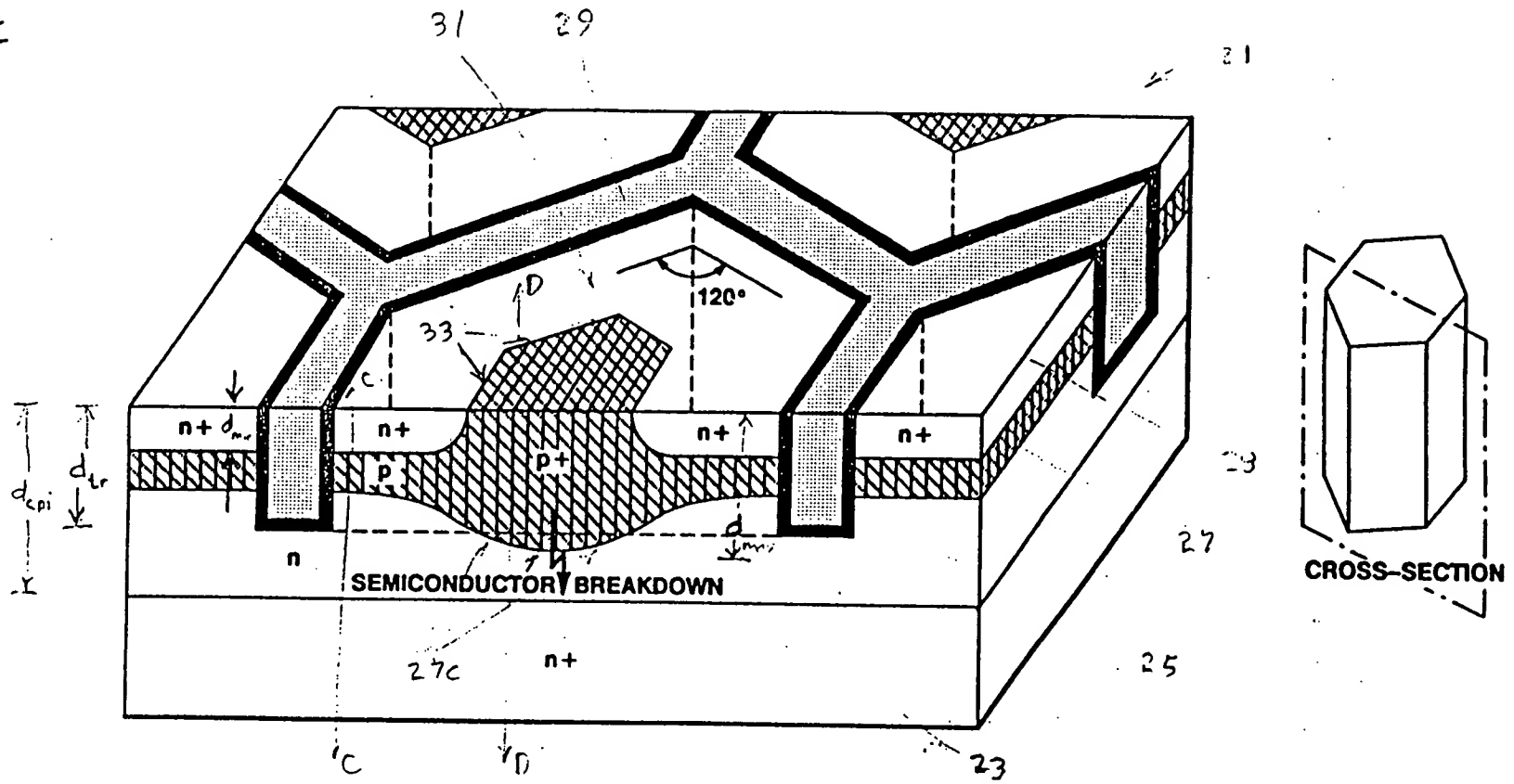
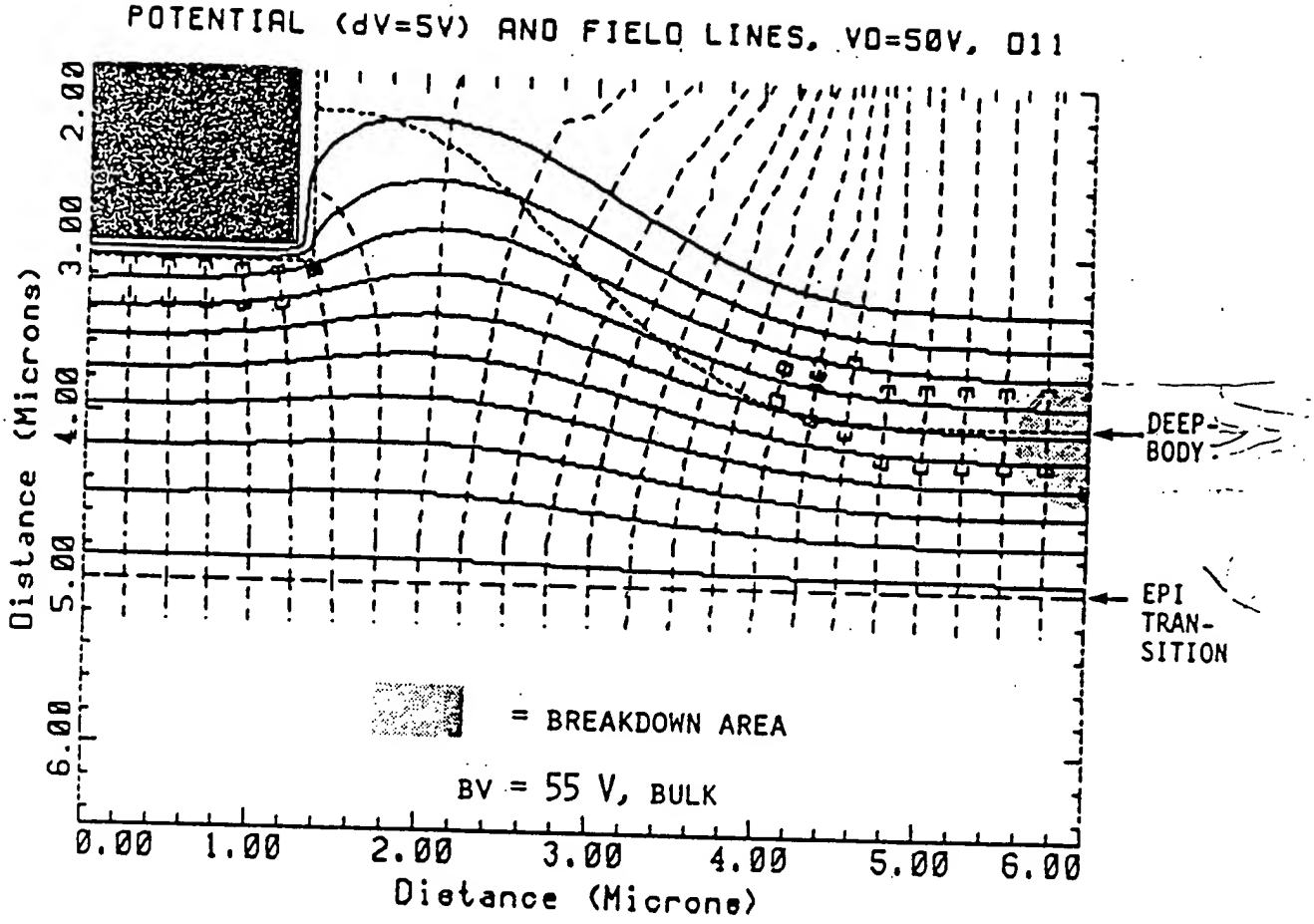


Figure 8

3-D representation of the optimized trenched DMOS transistor cell proposed in this Patent Application.



α_{eff} avalanche = 1 , α_{eff} = strong (exp) function of E

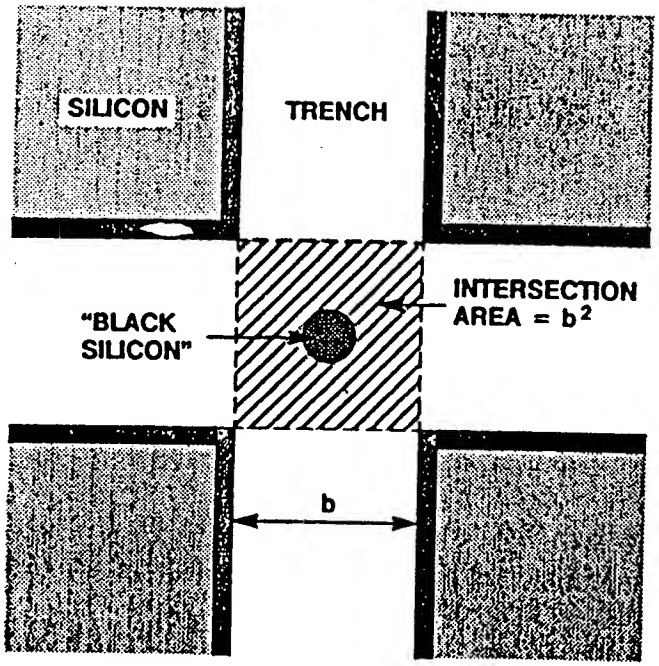
$$\alpha_{eff} = A E e^{-B/E}$$

Figure 9

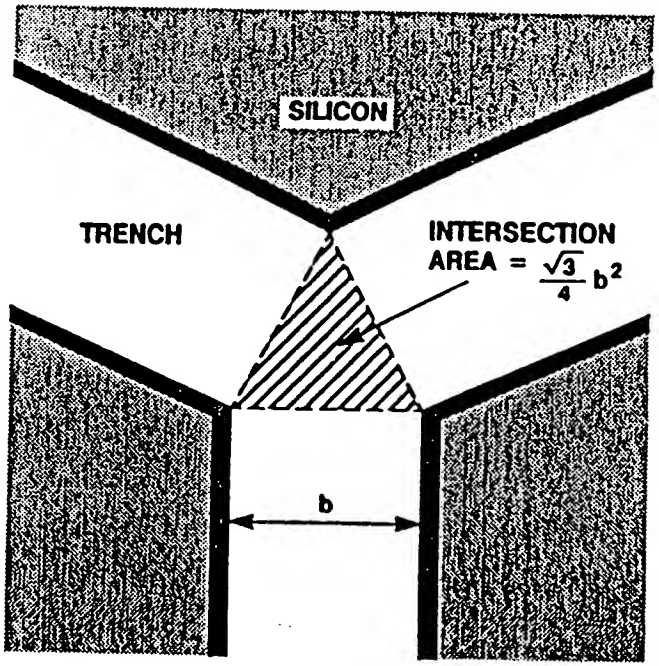
2-D computer simulation of the BVDSS operation of a trenched DMOS transistor having the deep body junction deeper than the trench. Drain breakdown takes place in the bulk.

read and understood August 10, 1988
read and understood August 4, 1988

"BLACK SILICON" COMPARISON



SQUARE CELLS



HEXAGONAL CELLS

Figure 10

Comparison of the "black silicon" areas at trench intersections: square cell (left) versus hexagonal cell (right).

read + understood August 10, 1988
read + understood Ralph D'Arrigo August 11, 1988

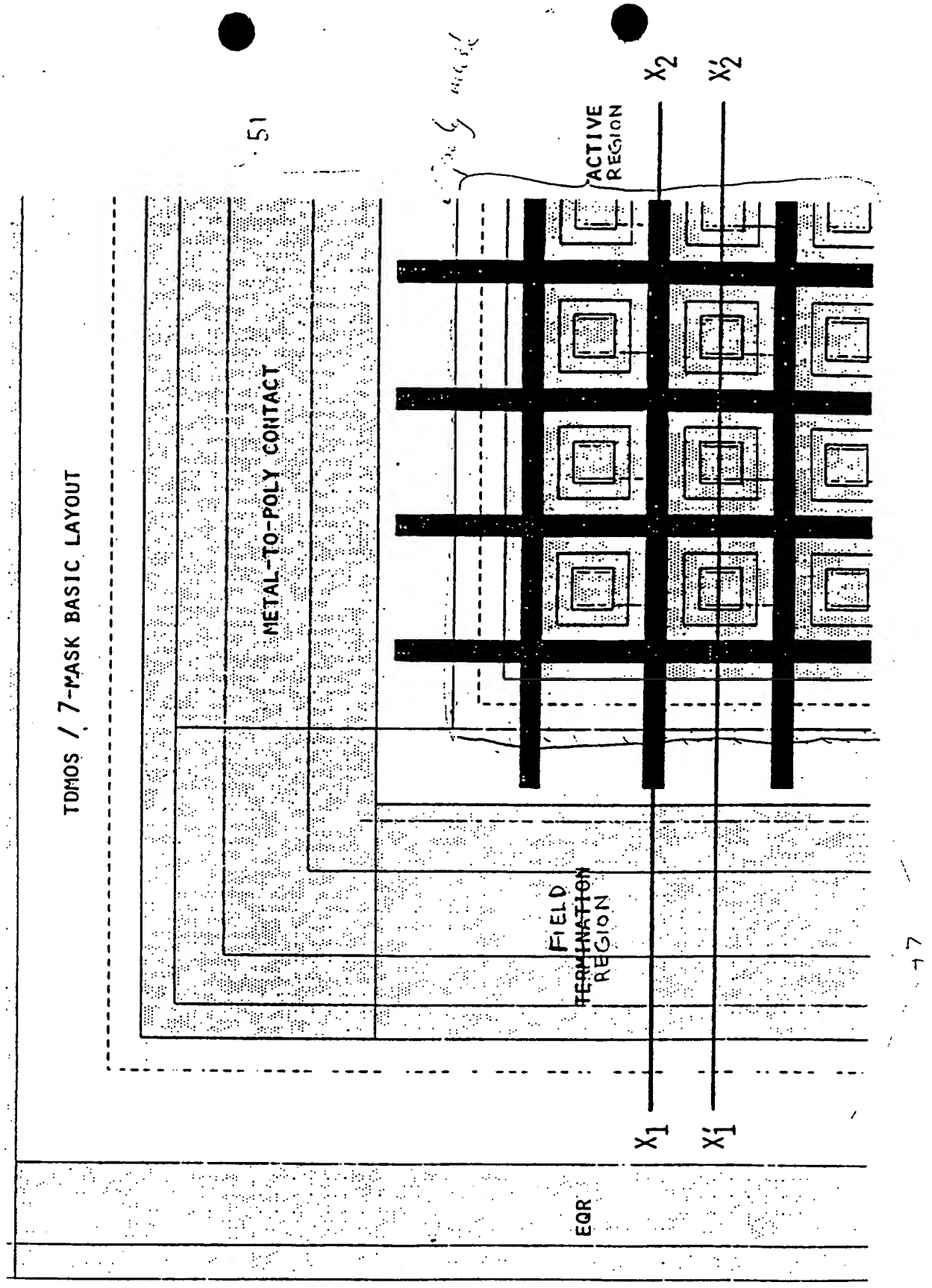


Fig. 21

read and understood RK Wall August 10, 1988
read and understood Randolph Hall August 11, 1988

0.6 μm

7-MASK TDMOS – PROCESSING BLOCK 1

n/n+ EPI ➡ POST-EPI OXIDATION ➡ MASK 1 = DEEP BODY ➡ BORON IMPLANT & DIFFUSION / OXIDATION ➡

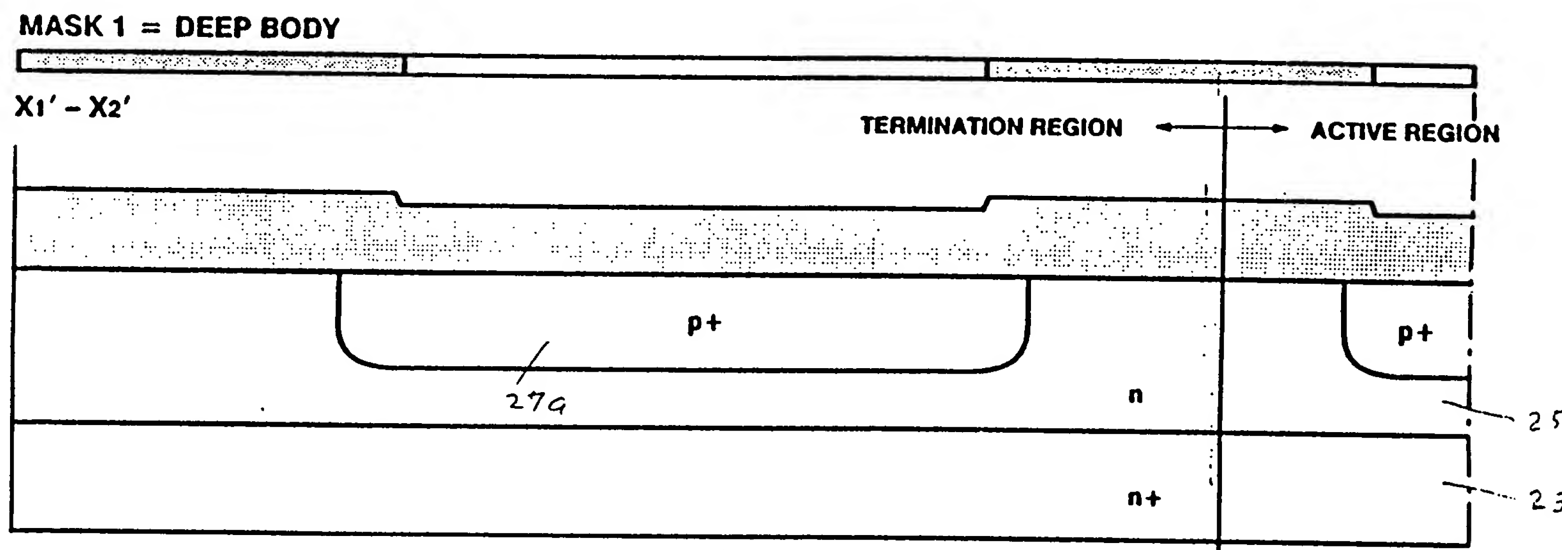


Fig. 22A

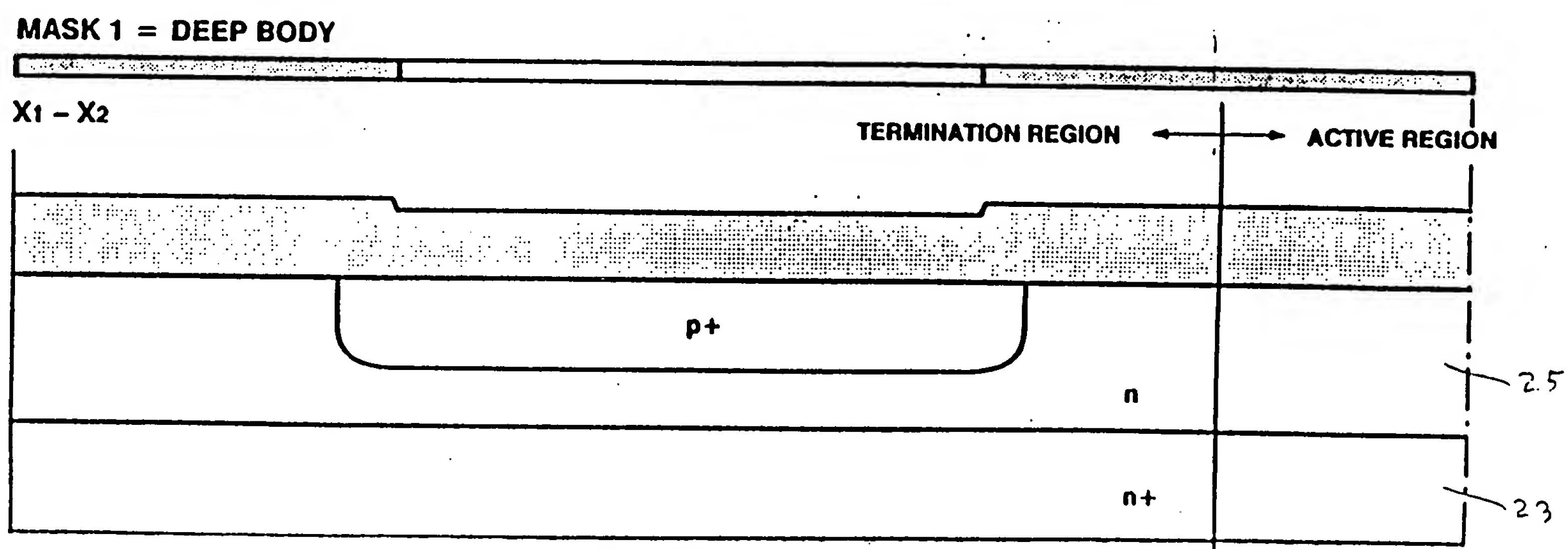


Fig. 22B

read and understood [signature] August 10, 1988
read and understood Randolph D. [signature] August 11, 1988

7-MASK TDMOS – PROCESSING BLOCK 2

➡ MASK 2 = ACTIVE ➡ BORON IMPLANT & DIFFUSION / OXIDATION ➡ ARSENIC IMPLANT & DIFFUSION / OXIDATION ➡ LTO DEPOSITION

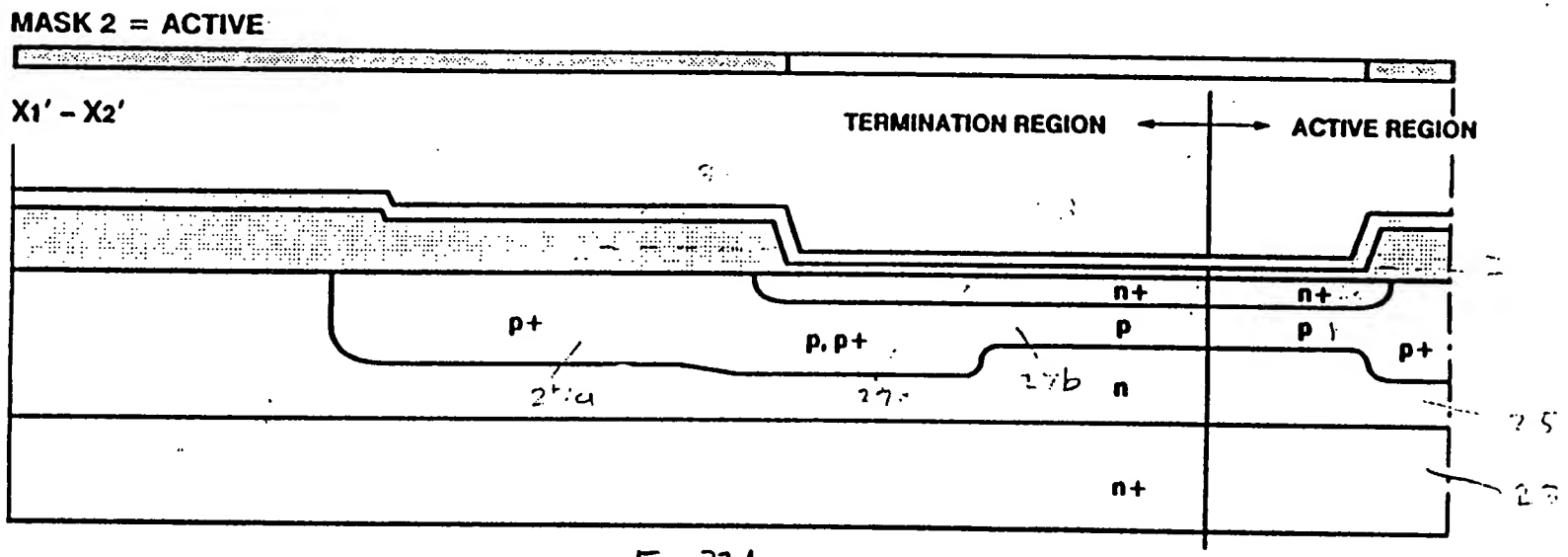
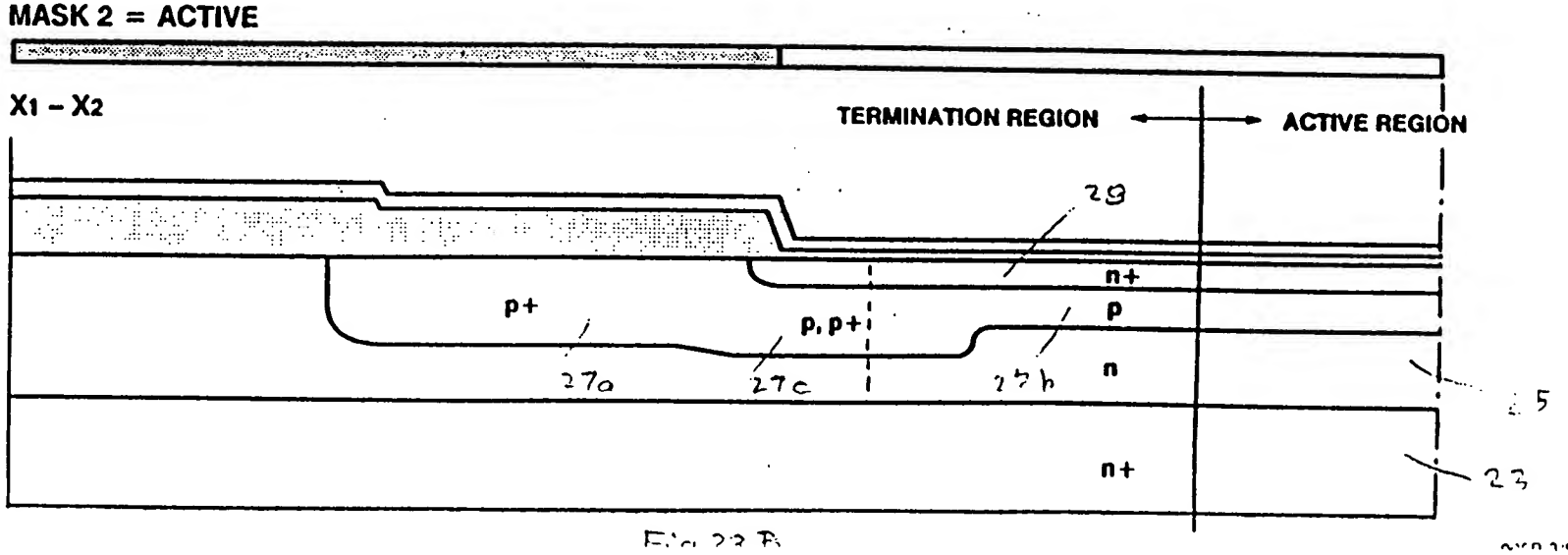


Fig. 23A



read & understood OK WH August 10, 1988
read & understood Ralph Dolan August 11, 1988

7-MASK TDMOS—PROCESSING BLOCK 3

MASK 6 = TRENCH → TRENCH DRY ETCHING

MASK 6 = TRENCH

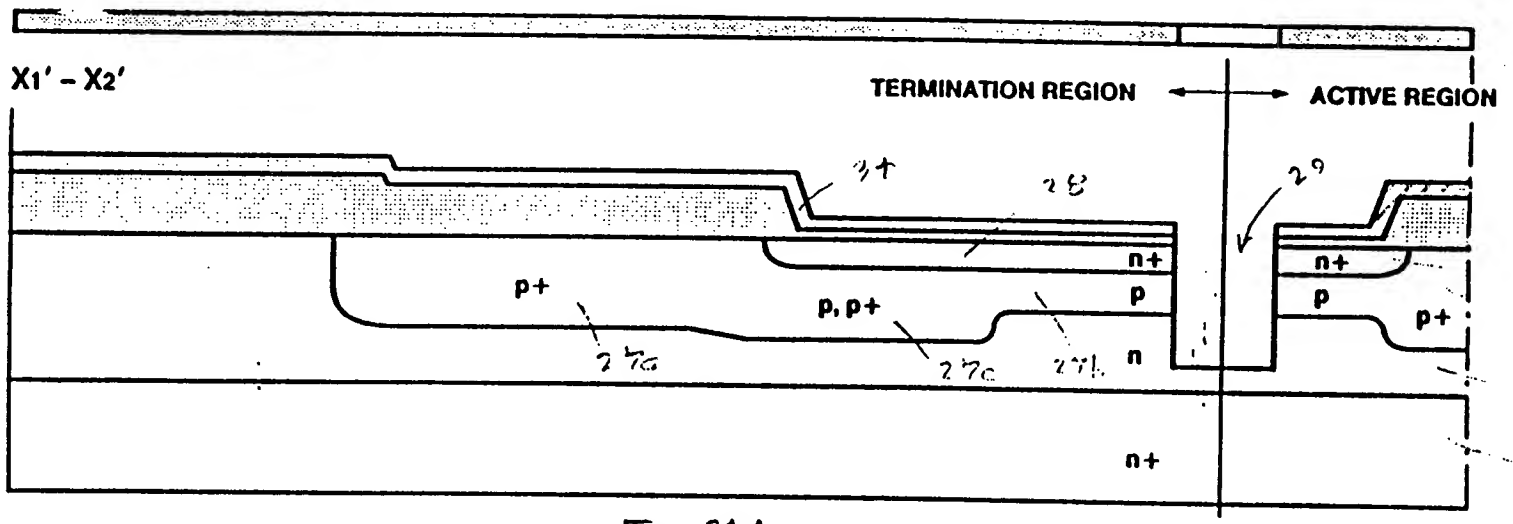
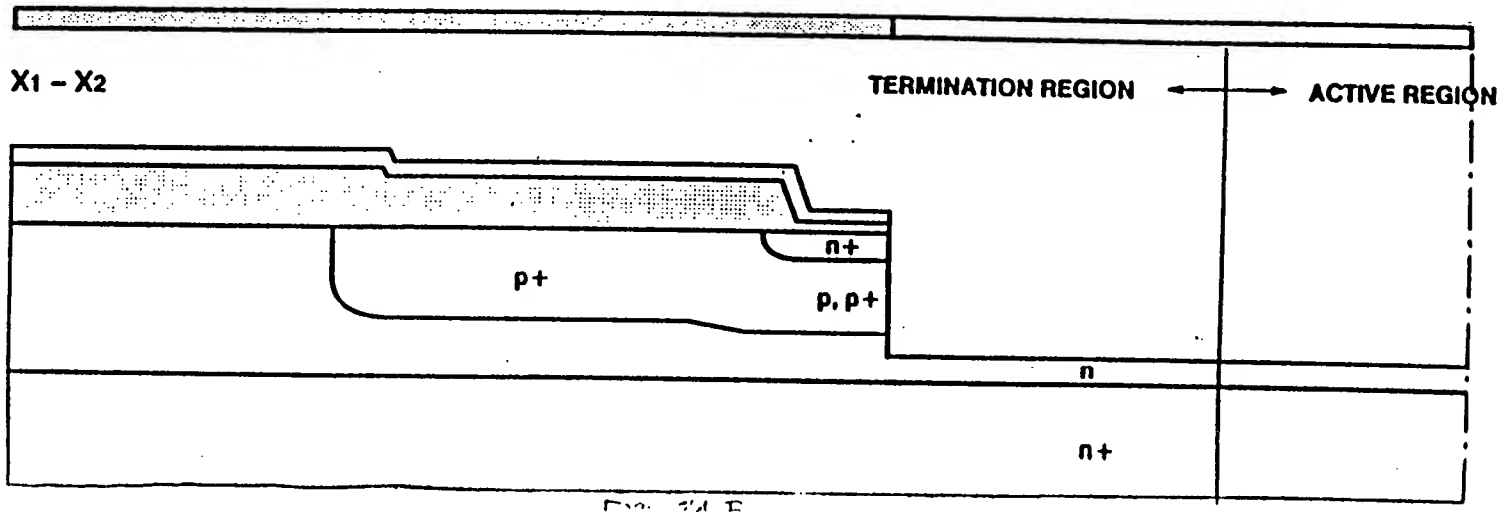


Fig. 24A

MASK 6 = TRENCH



7-MASK TDMOS – PROCESSING BLOCK 4

SACRIFICIAL OXIDATION & ETCHING → GATE OXIDATION →

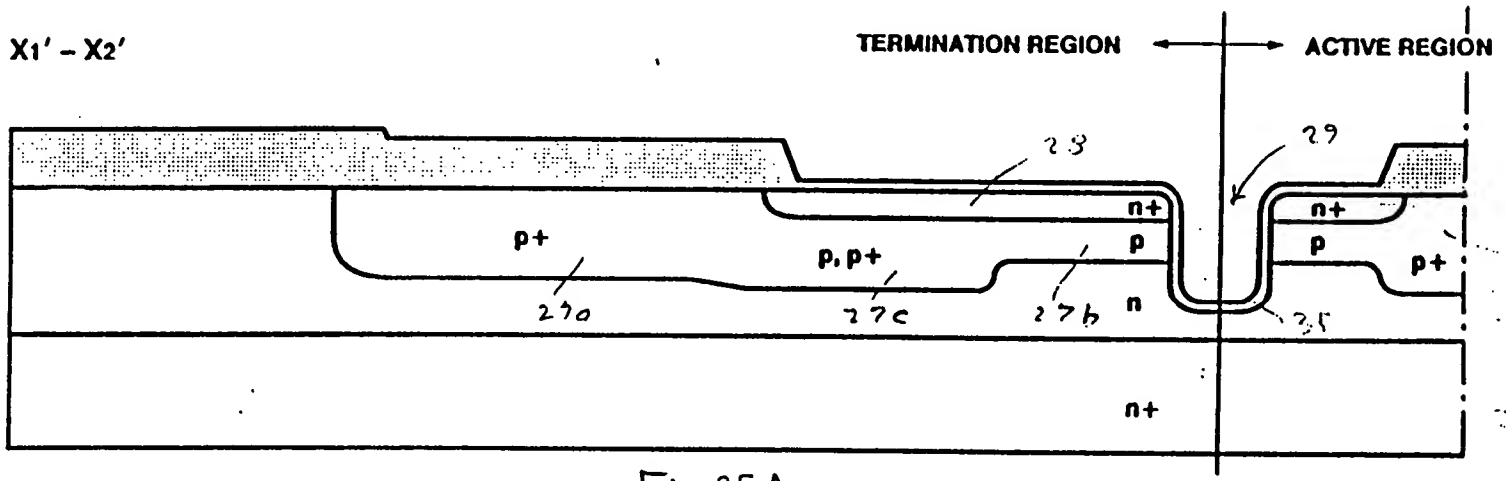


Fig. 25A

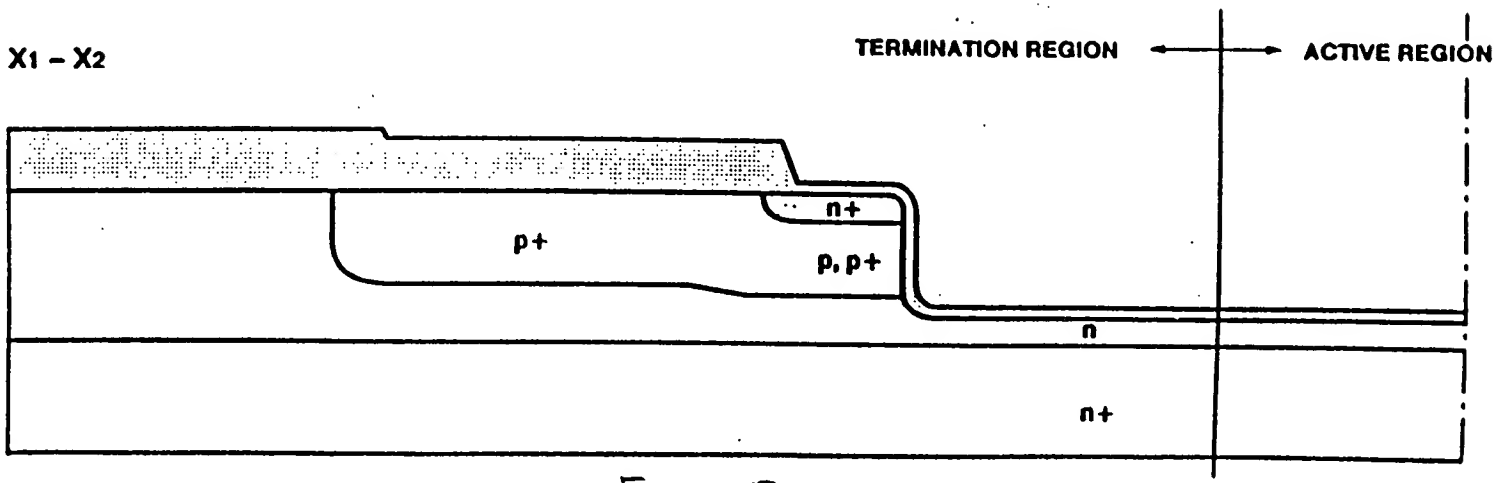


Fig. 25B

read & understood RKW August 10, 1988
read and understood Richard Rice August 11, 1988

7-MASK TDMOS—PROCESSING BLOCK 5

→ FIRST POLY DEPOSITION & PHOSPHORUS DOPING → OXIDATION (ETCH STOP) →

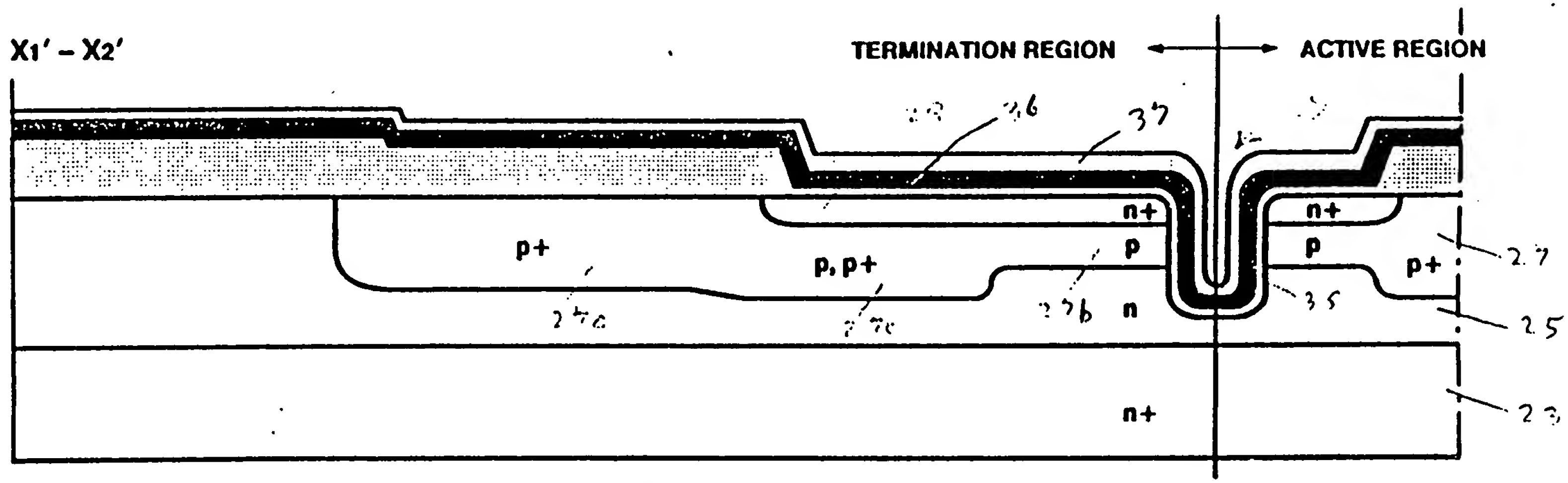


Fig. 26A

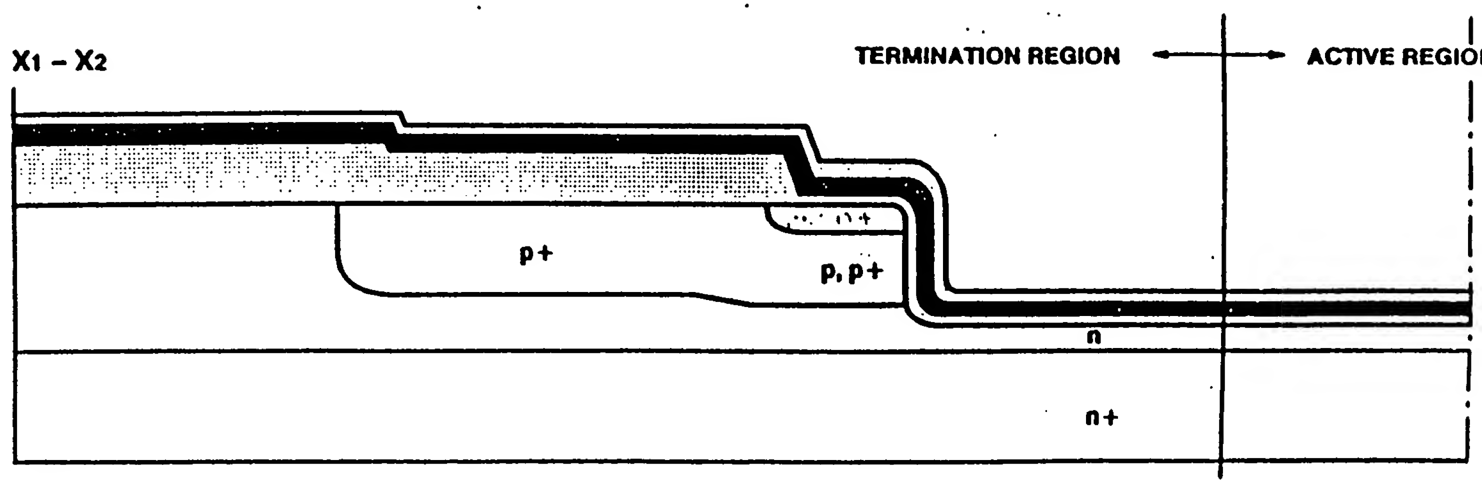


Fig. 26B

read & understood [signature] August 10, 1988
read and understood Rudolph D. [signature] August 4, 1988

7-MASK TDMOS—PROCESSING BLOCK 6

→ SECOND (UNDOPED) POLY DEPOSITION →

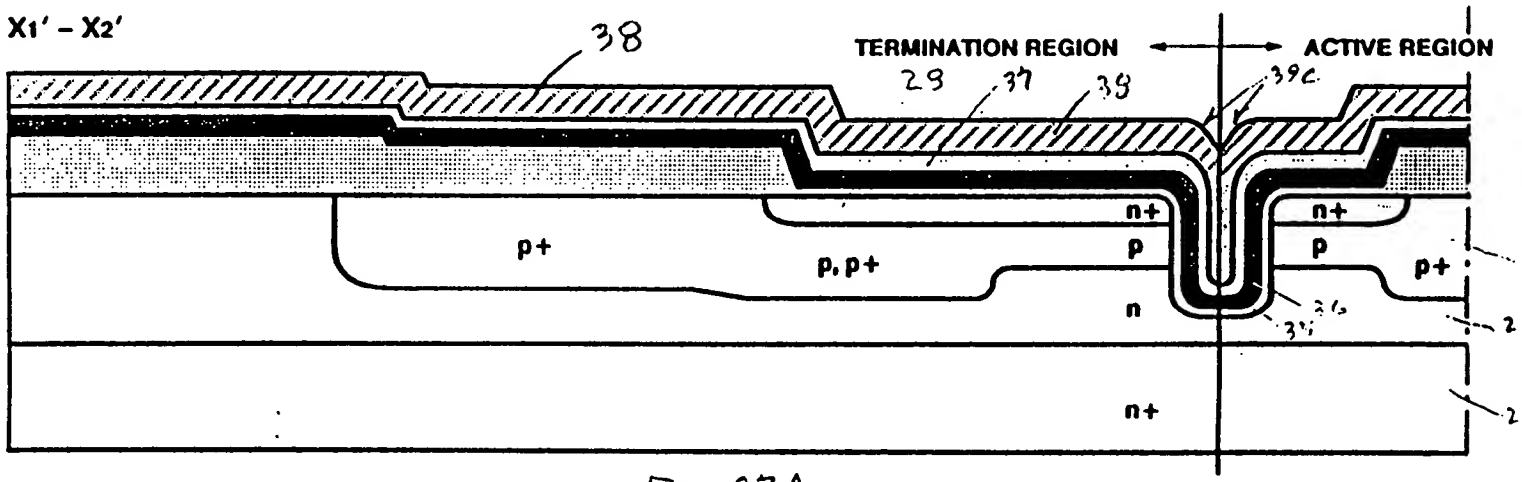


Fig. 27A

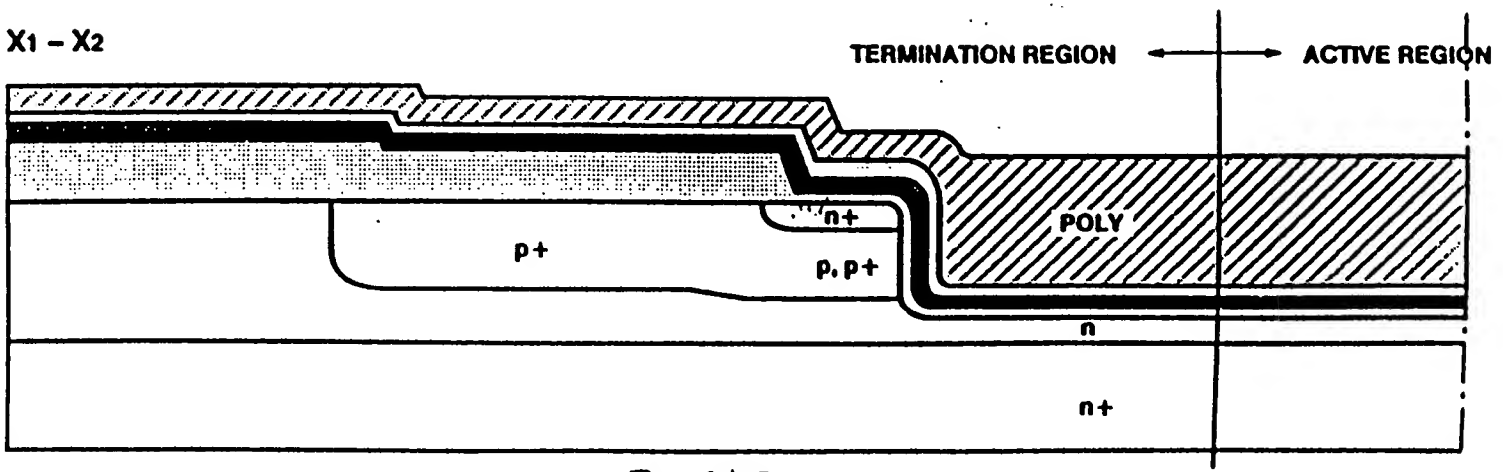


Fig. 27B

read + understood RKW August 10, 1988
read and understood Randall D. Kelly August 11, 1988

7-MASK TDMOS – PROCESSING BLOCK 7

POLY PLANARIZATION ETCHING → ETCH-STOP-OXIDE STRIP →

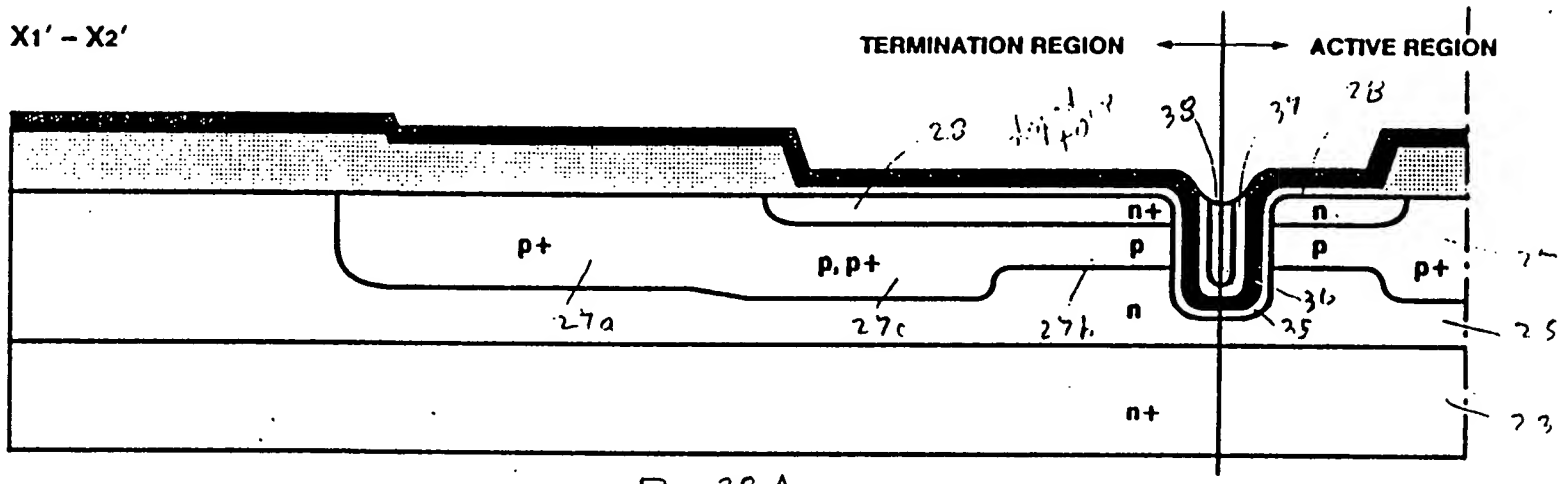


Fig. 28 A

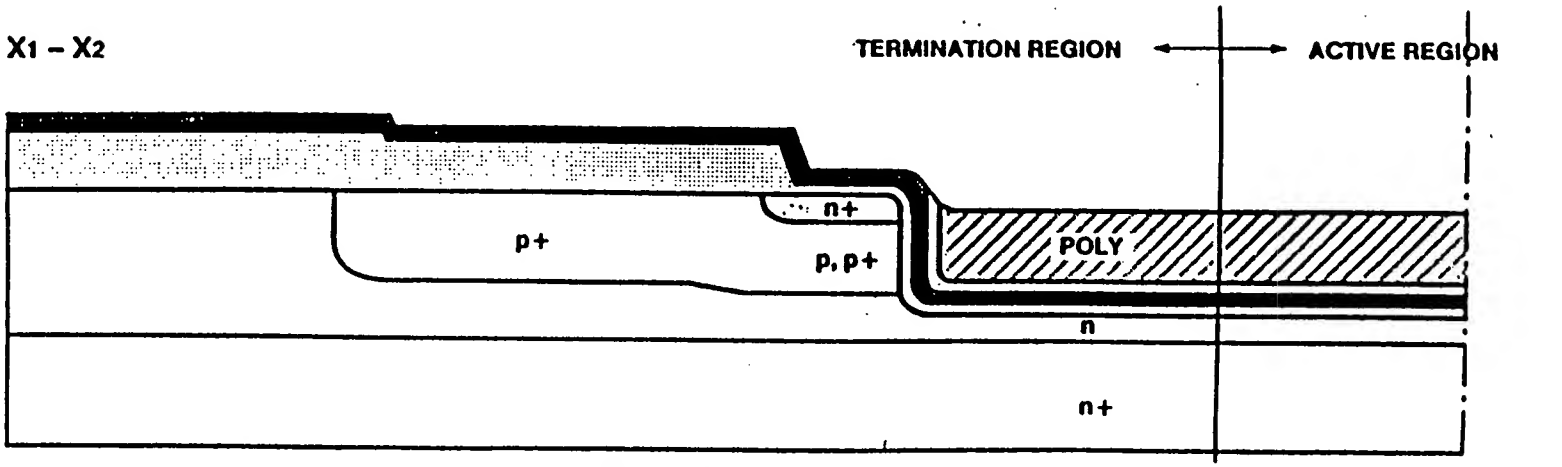


Fig. 28 B

7-MASK TDMOS—PROCESSING BLOCK 8

MASK 7 = POLY

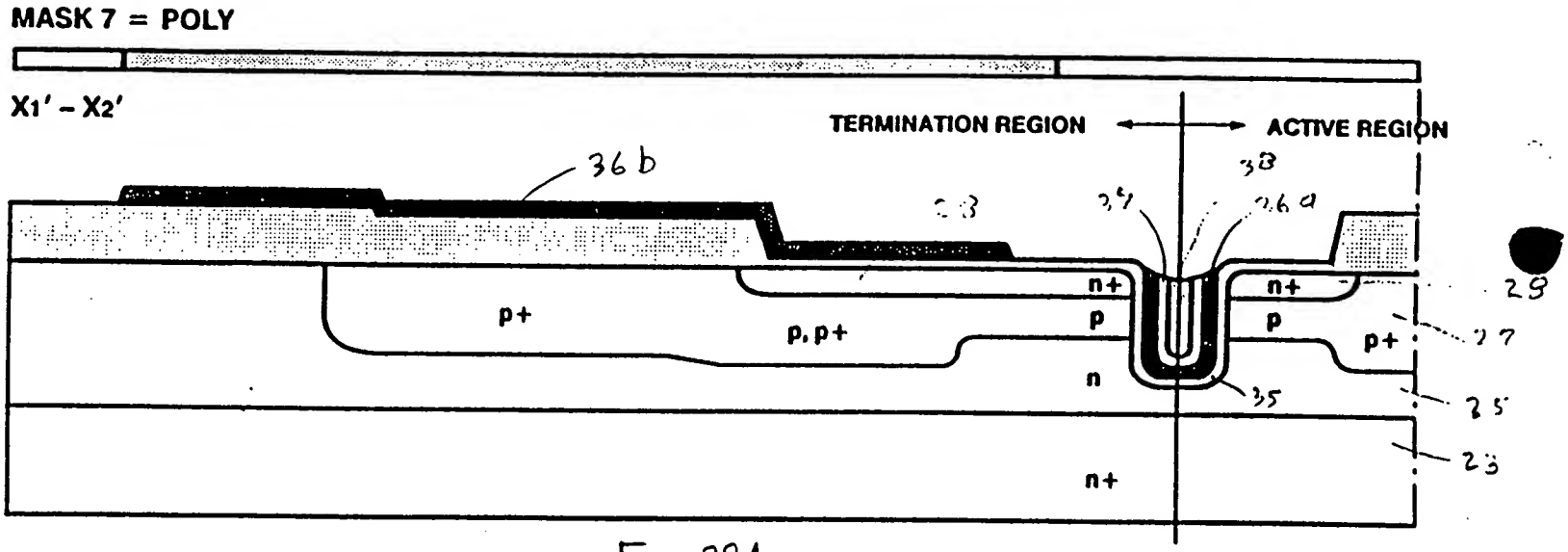


Fig. 29A

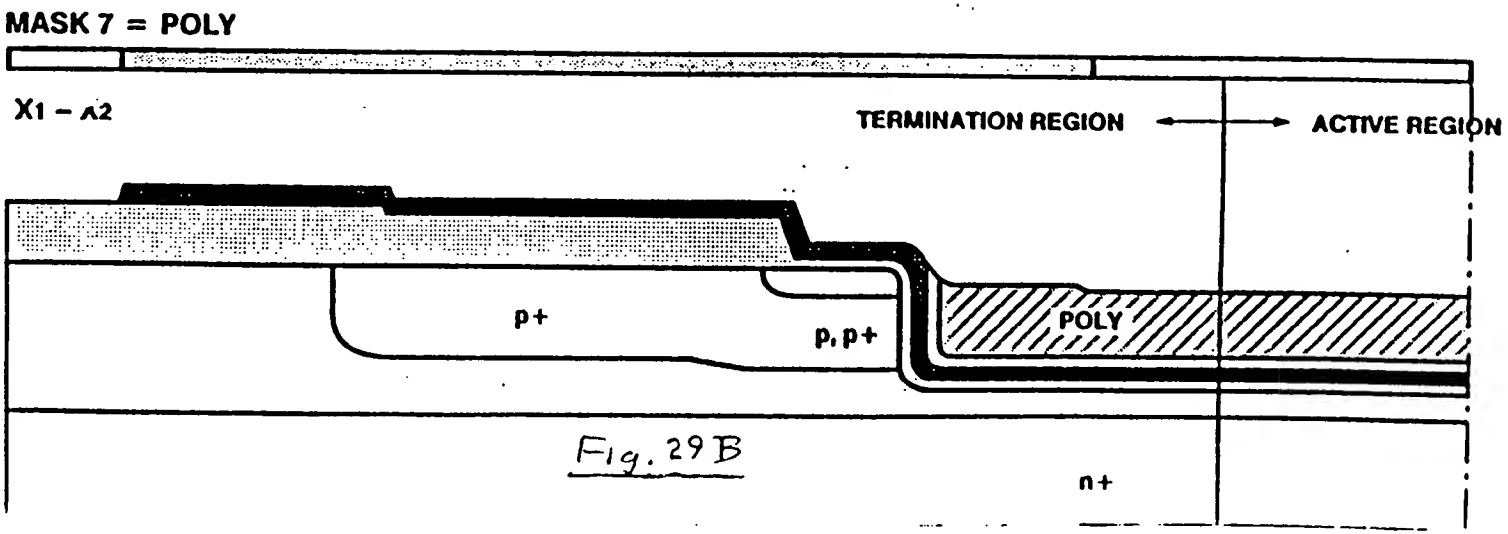


Fig. 29B

revised & updated August 10, 1988
Rail and updated Raleigh, NC August 11, 1988

7-MASK TDMOS—PROCESSING BLOCK 9

OXIDATION → BPSG DEPOSITION & FLOW → MASK 8 = CONTACT → BPSG REFLOW →

MASK 8 = CONTACT

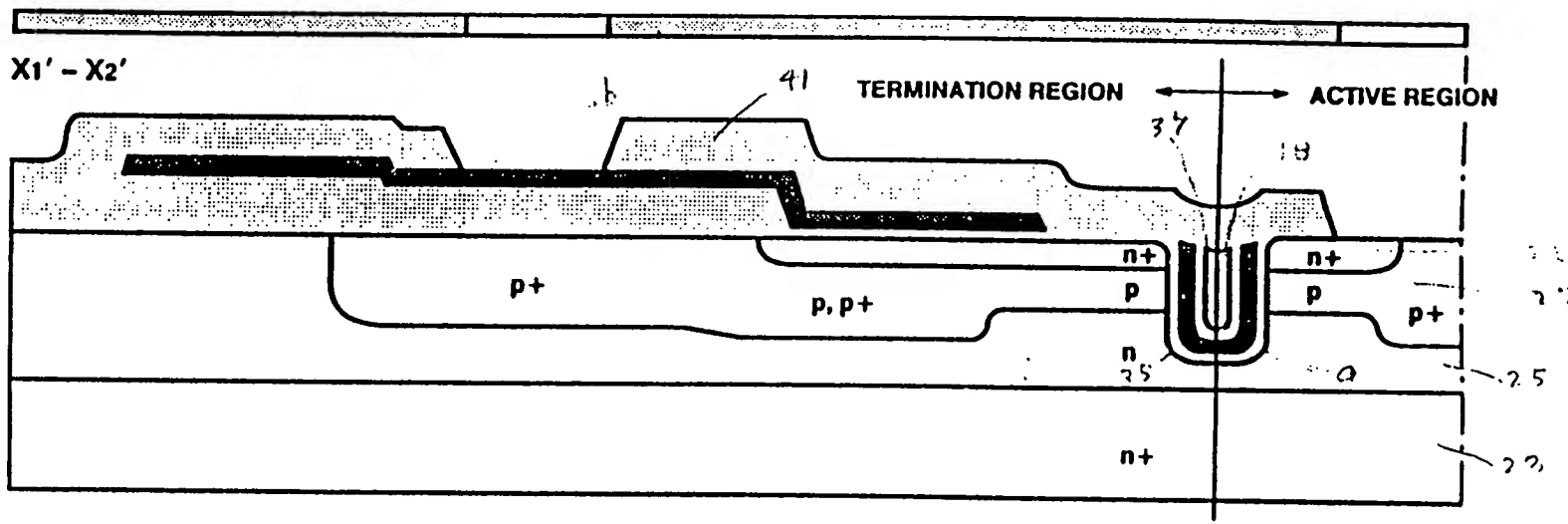
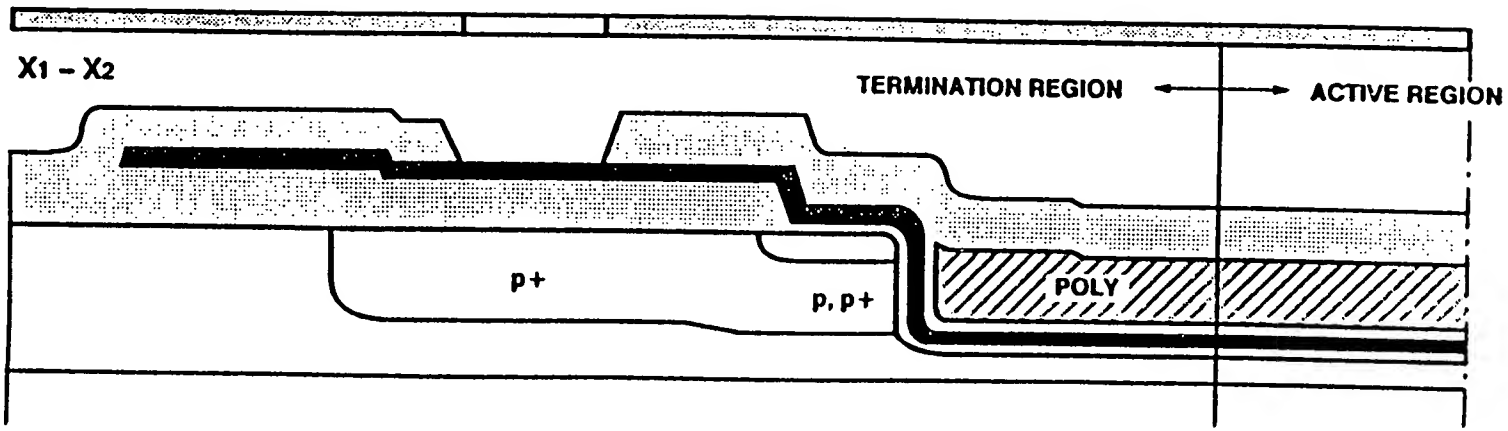


Fig. 30 A

MASK 8 = CONTACT



revised & updated August 10, 1988
and edited Randy D. Weil August 11, 1988

7-MASK TDMOS – PROCESSING BLOCK 10

ALUMINUM DEPOSITION → MASK 9 = METAL → METAL ALLOYING → ELECTRICAL CHECK →

MASK 9 = METAL

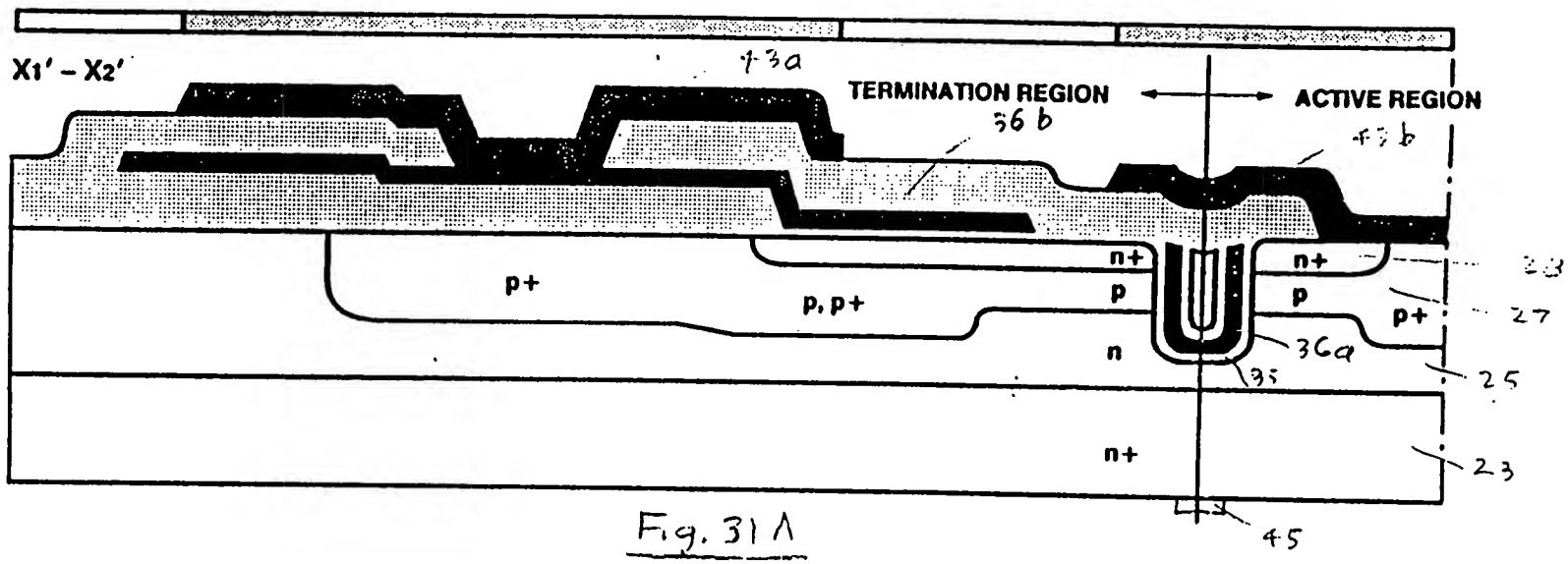
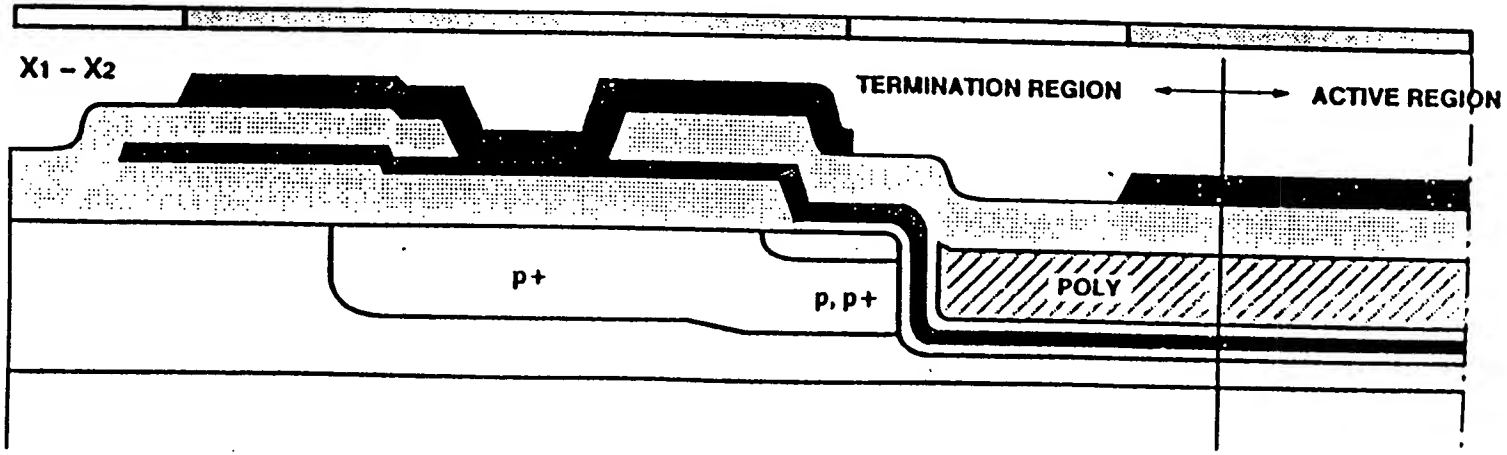


Fig. 31A

MASK 9 = METAL



read & understood GLK Aug 10, 1988
Neal and understood Randolph Neal August 4, 1988

EXHIBIT B

11-799

Siliconix
incorporated
2201 Laurelwood Road
Santa Clara, CA 95054
(408) 988-8000
TWX: 910-338-0227

3 October 1988

Mr. Paul J. Winters
Skjerven, Morrill, MacPherson, Franklin & Friel
3600 Pruneridge, Suite 100
Santa Clara, California 95051

Reference: Disclosure of Invention for TRENCHED DMOS POWER TRANSISTORS WITH OPTIMIZED DEEP-BODY PROFILE AND THREE-DIMENSIONAL GEOMETRY
Inventors: Constantin Bulucea and Rebecca Rossen

Dear Paul:

Please prepare a patent application for this invention for filing in the United States.

You will note that Constantin Bulucea has not specified his citizenship on the Invention Disclosure Form, but has shown his U.S. Resident Alien Number. He was born in Romania, but he says he is no longer Romanian.

Your files M-300, M-300/1, M-300/2, and M-584 may relate to this invention.

Very truly yours,

Siliconix incorporated

Lorimer K. Hill
Patent Coordinator

Enclosure:
Disclosure of Invention, dtd 11Aug88, 41 pp.